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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/592,349	06/12/2000	William C. Peatman	SC11100ZP	5118

23330 7590 04/29/2003

MOTOROLA, INC.
CORPORATE LAW DEPARTMENT - #56-238
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EXAMINER
WILLE, DOUGLAS A

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 04/29/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/592,349	PEATMAN ET AL.	
	Examiner	Art Unit	
	Douglas A Wille	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 February 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 4-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 4-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 2, 4, 5, 7 - 10 –13, 15, 16 and 19 - 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Abrokwah et al. ('929) in view of Kimura and Abokwah et al. ('739).

3. With respect to claim 1 Abrokwah et al. ('929) show a HFET (see cover Figure and column 2, line 41 et seq.) with a substrate 10 of GaAs with AlGaAs intermediate layers, with layer 16 of GaAs, delta doped layer 22, InGaAs channel layer 23, AlGaAs layer 24 and cap layer 25 of GaAs. There is a gate contact 30 with sidewalls 35 and the layer 25 is partly removed. Abrokwah et al. ('929) do not show the layer 22 is GaAs but it would have been obvious to form it with GaAs to show the required bandgap discontinuity with the channel layer and since it would be compatible with the GaAs layer beneath it. Note that since layer 22 is delta doped it will have some undoped material on either face. Note also that implantation is performed before the layer 25 is removed. Kimura shows a FET where the gate has a layer of i-GaAs which is the same width as the gate and provides high speed operation. It would have been obvious to apply the Kimura technique to the Abrokwah et al. ('929) device for the advantage shown (see abstract). Abrokwah et al. ('929) do not show the thickness of the GaAs layer but Abrokwah et al. ('739) show the thickness of layer 25 but Abrokwah et al. ('739) show a similar device in which the layer is < approximately 5 nm (column 2, line.21). It would have been obvious to use

this thickness since it is known to be functional and since criticality has not been established and since Abrokwah et al. ('739) use the modifier "approximately", it is regarded as equivalent to 6 nm.

4. With respect to claim 2, Abrokwah et al. ('929) do not show the thickness of layer 25 but Abrokwah et al. ('739) show a similar device in which the layer is < approximately 5 nm (column 2, line 21). With respect to claims 3 and 19, it would have been obvious to use this thickness since it is known to be functional and since criticality has not been established and since Abrokwah et al. ('739) use the modifier "approximately", it is regarded as equivalent.

5. With respect to claims 4 and 5, the substrate is exposed when the layer 25 is removed.

6. With respect to claim 7, Abrokwah et al. ('929) shows implantation before.

7. With respect to claim 8, Abrokwah et al. ('929) shows spacer formation after.

8. With respect to claim 9, Abrokwah et al. show spacer formation before removing a portion of the layer.

9. With respect to claim 10, Abrokwah et al. ('939) shows a third portion under the spacer.

10. With respect to claim 11, layer 22 of Abrokwah et al. ('939) is delta doped.

11. With respect to claim 12, Abrokwah et al. shows a support 11, a buffer 18, a delta doping layer 22 with an inherent spacer layer, a channel layer 23 and a barrier layer 24.

12. With respect to claim 13, there is a gate 30 in Abrokwah et al. ('939).

13. With respect to claim 15, a first portion remains under the gate and there is no change to the doping.

14. With respect to claims 16 and 20, Abrokwah et al. ('929) show a HFET (see cover Figure and column 2, line 41 et seq.) with a substrate 10 of GaAs with AlGaAs intermediate

layers, with layer 16 of GaAs, delta doped layer 22, InGaAs channel layer 23, AlGaAs layer 24 and cap layer 25 of GaAs. There is a gate contact 30 with sidewalls 35 and the layer 25 is partly removed. Abrokwah et al. ('929) do not show the layer 22 is GaAs but it would have been obvious to form it with GaAs to show the required bandgap discontinuity with the channel layer and since it would be compatible with the GaAs layer beneath it. Note that since layer 22 is delta doped it will have some undoped material on either face. Note also that implantation is performed before the layer 25 is removed. Kimura shows a FET where the gate has a layer of i-GaAs which is the same width as the gate and provides high speed operation. It would have been obvious to apply the Kimura technique to the Abrokwah et al. ('929) device for the advantage shown (see abstract). Abrokwah et al. ('929) do not show the thickness of the GaAs layer but Abrokwah et al. ('739) show the thickness of layer 25 but Abrokwah et al. ('739) show a similar device in which the layer is < approximately 5 nm (column 2, line 21). It would have been obvious to use this thickness since it is known to be functional and since criticality has not been established and since Abrokwah et al. ('739) use the modifier "approximately", it is regarded as equivalent to 6 nm. Also, Abrokwah et al. shows a support 11, a buffer 18, a delta doping layer 22 with an inherent spacer layer, a channel layer 23 and a barrier layer 24.

15. With respect to claim 19, Abrokwah et al. ('929) do not show the thickness of layer 25 but Abrokwah et al. ('739) show a similar device in which the layer is < approximately 5 nm (column 2, line 21). It would have been obvious to use this thickness since it is known to be functional and since criticality has not been established and since Abrokwah et al. ('739) use the modifier "approximately", it is regarded as equivalent.

16. With respect to claim 21, it would have been obvious to anneal the structure to remove any damage due to the etching process.

17. Claims 6 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Abrokwah et al. ('929) in view of Kimura and Abokwah et al. ('739) and further in view of Hara et al.

18. Abrokwah et al. ('929) shows implantation before removal but Hara et al. shows (see Figure 6 and 7 and column 7, line 24) that for a FET structure the implantation can be performed either before or after removal as a design consideration and it would be obvious to perform the implantation either before or after.

19. With respect to claims 6 and 14, implantation after is shown as an alternative and Abrokwah et al. ('939) show S/D contacts 45/46 and it would have been obvious to anneal the structure to remove any damage due to implantation.

20. Claims 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Abrokwah et al. ('929) in view of Kimura, Abokwah et al. ('739) and further in view of Hara et al. and Abrokwah et al. ('285).

21. Abrokwah et al. ('285) show a similar device (see cover Figure) with a double layer sidewall. It would have been obvious to use the double layer sidewall shown by Abrokwah et al. ('285) as an implant mask (column 4, line 63) in the Abrokwah et al. ('929) and Kimura device as a design choice. With respect to claim 17, Abrokwah et al. ('285) show implanting after removal and it would have been a design choice to remove the layer either before or after implanting with appropriate adjustment of the implant parameters. Note that if the spacer is not

needed as a mask for implantation it could be applied at any time including both before and after implantation.

Response to Arguments

22. Applicant's arguments filed 3/27/02 have been fully considered but they are not persuasive.

23. Applicant misunderstands advantage and suggests nonsense alternatives and no further comment is provided.

24. Applicant states that there is no reason to combine the references with respect to claims 1 and 16 but reasons are given.

25. Applicant states that about 5 is not the same as 6 but ignores the fact that criticality is not established and the mere slight change of a parameter does not make an unpatentable invention patentable.

Conclusion

26. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Douglas A Wille whose telephone number is (703) 308-4949. The examiner can normally be reached on M-F (6:15-2:45).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmi can be reached on (703) 308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

LONG PHAM
PRIMARY EXAMINER

DAW
April 25, 2003